

Digital Implementation of Adaptive Voltage Position (AVP) for Voltage Regulator Module (VRM)

Li Ma, Ming Xu, Alex Q. Huang

Center for Power Electronics Systems
The Bradley Department of Electrical and Computer Engineering
Virginia Polytechnic Institute and State University
Blacksburg, VA 24061 USA

Abstract— This paper compares two digital implementation methods to achieve adaptive voltage position (AVP) for voltage regulator module (VRM). One is the peak current control method, and the other one is the active droop method. The key to the digital implementation is the A/D converter in the current loop. For peak current control method, the required ADC sampling frequency is much higher than that for active droop method. A new digital implementation using double-edge modulation is investigated and shows its benefit in terms of cost.

I. INTRODUCTION

Digital control for voltage regulator module (VRM) draws more and more attention recently, due to its advantages on noise immunity, design flexibility and ease of integration with other digital parts in the system.

Adaptive voltage position (AVP) is a necessary function for VRM control design. The basic idea to achieve AVP is to design the output impedance of the VRM to be a constant value [1]. Fig. 1 shows the method of constant output impedance to achieve AVP, where V_{VID} is determined by system VID value, R_{droop} is the droop resistor which is determined by Intel's load line specification. Therefore, the relationship of output voltage V_o and V_{max} can be derived as

$$V_o = V_{max} - I_o \cdot R_{droop} \quad (1)$$

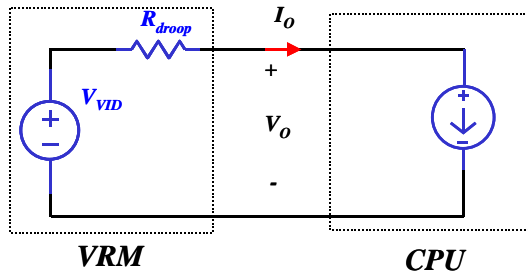


Fig. 1 Constant output impedance to achieve AVP

There are mainly two ways to achieve constant output impedance of VRM, one is to use peak current control, and the other one is to use active droop control.

Peak current control method is introduced and its digital implementation is discussed in section II. In section III, active droop control method is investigated and its digital implementation is compared with the peak current mode control. In section IV, double-edge modulation is investigated to further reduce the sampling frequency of ADC in current loop.

II. DIGITAL IMPLEMENTATION OF PEAK CURRENT CONTROL TO ACHIEVE AVP

The architecture of peak current mode control for VRM is shown in Fig.2. Fig. 3 is its equivalent small signal model [2].

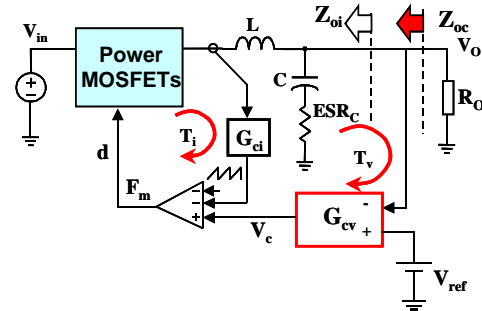
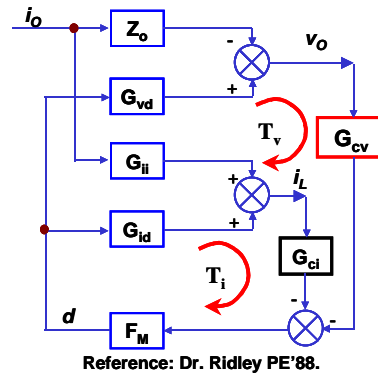


Fig. 2 Architecture of peak current mode control to achieve AVP



Reference: Dr. Ridley PE'88.
Fig. 3 Small signal model of peak current control

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G_{ci} is the compensation transfer function in current loop, which consists of sensing resistance and transconductance

(g_m) of sensing g_m amplifier. G_{cv} is the compensation transfer function in voltage loop. Z_{oi} is the output impedance with only current loop closed, Z_{oc} is the output impedance with both voltage loop and current loop closed. The design issue is to choose G_{cv} to make Z_{oc} equal to R_{droop} . The basic idea is to make V_c , which is the output of G_{cv} , change proportionally with load current I_o . For example, as I_o changes from a small value to a big value (shown in Fig. 4), V_c also changes from a very small value to a bigger value due to the amplification function of G_{cv} . At this time, V_o reduces a little, but the reduction of V_o is so small that it has almost no influence to the rising slope of inductor current, which is determined by $(V_{in}-V_o)/L$. However, V_c increases a lot. Therefore, the duty ratio at this time is increased to support heavier load current. How to choose correct G_{cv} can be referred to [1] and is not further discussed in this paper. Fig. 5 shows simulation results of AVP for a two-channel 1.25V/40A VRM using peak current control.

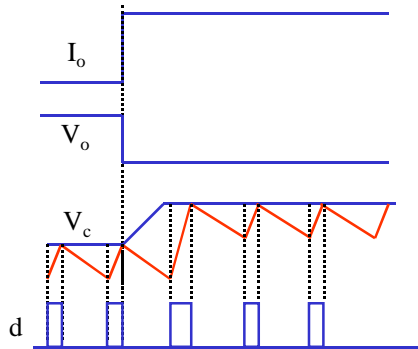


Fig. 4 Illustration of transient response

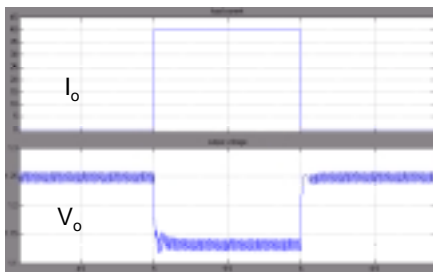


Fig. 5 Simulation results of AVP with a two-channel 1.25V/40A VRM using peak current control

According to Fig. 5, peak current control can achieve very good AVP function, however, it is noise sensitive. It should be very careful to choose G_{cv} . A filter is needed to get rid of the switching frequency noise. Another issue is that G_{cv} has finite gain, which results an offset voltage at light load condition. Digital implementation of peak current control has higher noise immunity. The architecture is shown in Fig. 6. It needs at least two ADCs. One is for the current loop, the other one is for the voltage loop. Since the voltage loop and current loop are coupled together, it is difficult to use direct design method [2]. In this paper, redesign method is used to implement AVP.

For peak current mode control, the speed of ADC_i in current loop should be high enough to catch the peak current point, otherwise, the sample and hold effect of ADC_i will make the transient response much worse. Fig. 7 shows the simulation results of transient response of digital implementation for peak current control to achieve AVP using the ADC_i whose sampling frequency is 20 times switching frequency (a) and the ADC_i whose sampling frequency is 100 times switching frequency (b).

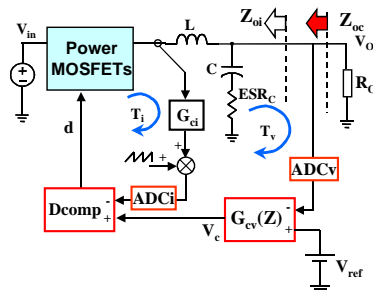
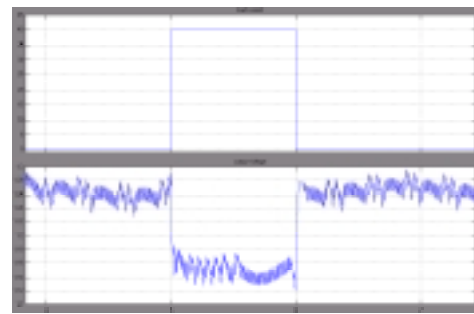
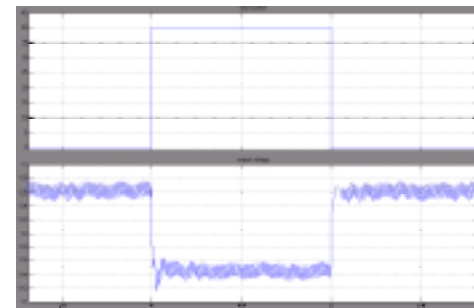


Fig. 6 Architecture of digital implementation of peak current control



ADCi: $f_{sample} = 20f_{sw}$
(a) Sampling frequency of ADC_i is 20 times of switching frequency



ADCi: $f_{sample} = 100f_{sw}$
(b) Sampling frequency of ADC_i is 100 times of switching frequency

Fig. 7 Simulation results of digital implementation of peak current control to achieve AVP for a two-channel 1.25V/40A VRM

Fig. 8 shows the sample and hold effect of ADC_i with sampling frequency of 20 times switching frequency. The sensed inductor current plus an external ramp is compared with the control signal V_c . The analog i_L signal is sampled to generate the digitized i_L signal. Due to the sample and hold effect, the comparison with V_c generates duty cycle errors

both in steady state and in transient. To reduce the impact of sample and hold effect, the direct method is to increase the sampling frequency, resulting in using high cost ADC.

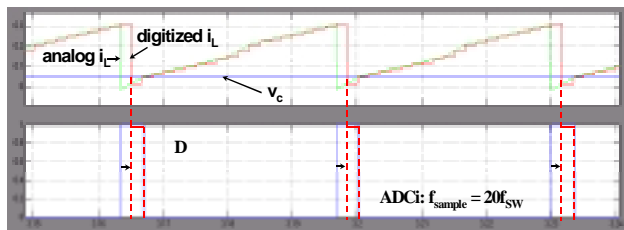


Fig. 8 Simulation results of sample and hold effect of ADC

III. DIGITAL IMPLEMENTATION OF ACTIVE DROOP CONTROL TO ACHIEVE AVP

The fundamental idea of active droop control is to change the voltage reference, so that it increases or decreases as load current decreases or increases. The compensator is just designed to follow the change of voltage reference. The architecture is shown in Fig. 9. Fig. 10 illustrates the basic idea of active droop control.

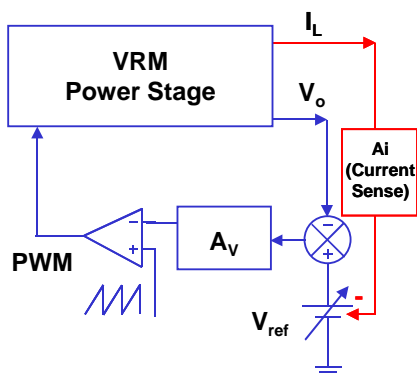


Fig. 9 Architecture of active droop control to achieve AVP

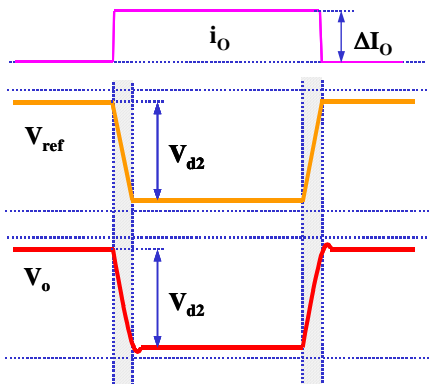


Fig. 10 Illustration of basic idea of active droop control to achieve AVP

Compared with peak current control, the compensator A_v of active droop control can have infinite gain. Therefore, there is no offset voltage at light load condition. How to

design A_v can be referred to [1], and is not discussed in this paper. Fig. 11 shows the simulation results of AVP using active droop control for a two-channel 1.3V/40A VRM.

The architecture of corresponding digital implementation is shown in Fig. 12. Only one ADC is used. The design of A_v impacts both voltage loop and current loop. So, the redesign method is used.

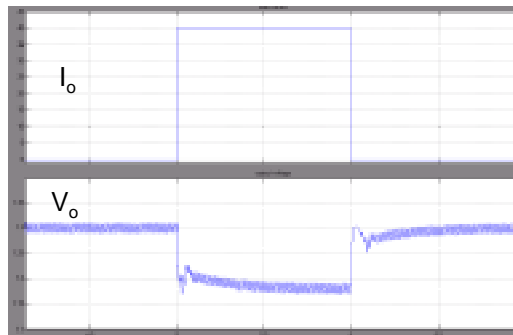


Fig. 11 Simulation results of AVP using active droop control for a two-channel 1.3V/40A VRM

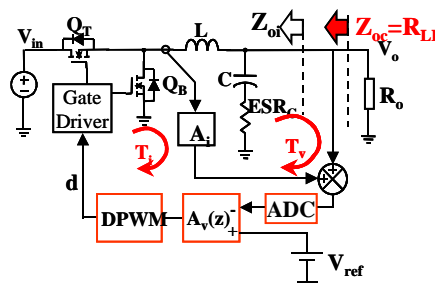


Fig. 12 Architecture of digital implementation of active droop control to achieve AVP

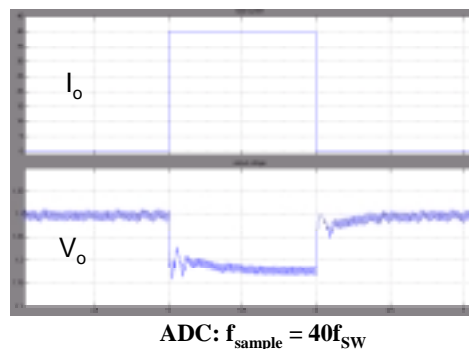


Fig. 13 Simulation results of digital implementation of active droop control to achieve AVP for a two-channel 1.3V/40A VRM

According to the design method of A_v , it averages its input signal. Therefore, there is no need for ADC to catch the peak current point, and the sample and hold effect has less influence. Fig. 13 shows the simulation results of digital implementation using ADC whose sampling frequency is 40 times the switching frequency.

Although the sampling frequency of ADC is greatly reduced, if active droop control is used, it is still a stringent requirement considering 1MHz switching frequency. The cost for this ADC is still high. To further reduce the sampling frequency of ADC, double-edge modulation is investigated.

IV. DIGITAL IMPLEMENTATION OF ACTIVE DROOP CONTROL TO ACHIEVE AVP

According to equation (1), if the load current can be accurately sensed, AVP can be achieved very easily. In peak current control and active droop control, normally inductor current is sensed, which has high frequency ripple, making the design tough. However, the average value of inductor current is exactly the load current. If the average inductor current can be sensed accurately, AVP design can be simplified. Therefore double-edge modulation [3] can be used to do the middle point inductor current sensing. Fig. 14 illustrates the average current sensing method using double edge modulation.

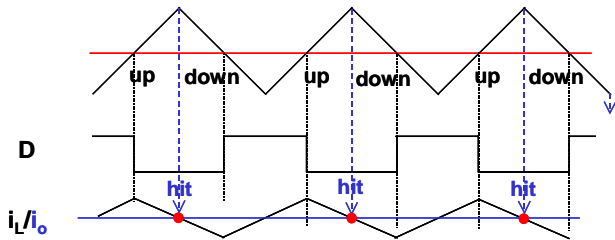


Fig. 14 Average inductor current sensing using double-edge modulation

The basic idea is that instead of using saw-tooth carrier signal for PWM comparator, triangle carrier signal is used. This triangle waveform is compared with the control signal, which ideally is a straight line, and the duty ratio is generated accordingly. Each edge of the duty cycle signal is determined by the crossing point of the control signal and the triangle carrier signal. If this triangle signal is equilateral, its peak point corresponds to the middle point of inductor current, which is equal to the load current. Then this current information can be used to design AVP easily.

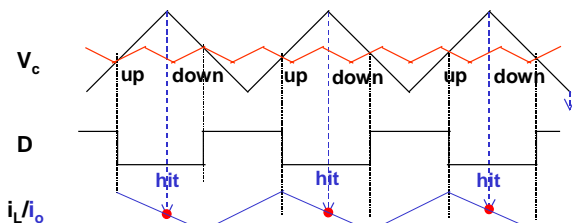


Fig. 15 A shift from middle point of inductor current happens when control signal has high frequency ripple

However, in real case, the control signal is not a ideal straight line, it has some high frequency ripple, which makes the crossing point uneven, resulting in a shift from middle point of inductor current (shown in Fig. 15). Although filters

can be used to reduce this high frequency ripple, they also limit the bandwidth of the closed loop system.

However, this problem can be solved by digital implementation. The feedback output voltage signal can be sampled at N times switching frequency, where N is the VRM channel number. Then the high frequency ripple cannot be introduced into the compensator, therefore, the control signal can be a strait line. In this way, the sampling frequency for inductor current can be reduced to switching frequency. This research work is on going and new results will be presented in the future.

V. CONCLUSION

Digital implementation of peak current control and active droop control to achieve AVP is discussed. The key part is the A/D converter in the current loop. For peak current control method, the sampling frequency of the ADC should be high enough, such that it can catch the peak current point. Therefore, the sample and hold effect has significant influence for this implementation. For active droop control, which is actually average current control, although the sampling frequency is greatly reduced compared with peak current control, it still should be 20 times the highest frequency of the sensed current waveform. The basic reason that ADC in current loop should have high sampling frequency for active droop method is that it cannot sense the average inductor current accurately. Therefore, a new digital implementation using double-edge modulation is proposed. The ADC sampling frequency in current loop is expected to be reduced to switching frequency. This research work is on going and new results will be presented in the future.

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