

Impacts of Transient Voltage Clamp on CPU Power Delivery

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Abstract— Transient Voltage Clamp (TVC) can be used in modern microprocessor power delivery loop to reduce passive decoupling elements. Where to put the TVC and how to control it are the objects of this paper. A microprocessor power supply design without bulk cap on motherboard by using TVC is proposed, which offers Adaptive Voltage Position function and can meet Intel’s VRD10.0 specifications.

Keywords- Transient Voltage Clamp; power delivery; AVP.

I. INTRODUCTION

The consequence of integrating more transistors into microprocessor for more powerful function is more power consumption. Today, power and power supply noise are increasingly becoming the dominant limiters to processor performance and cost [1]. The system designers not only need to deal with high current rating issue but also need to treat di/dt issue. With each generation of processor, di (transistor number) increases and dt (clock period) decrease, resulting an increase in supply noise. A current with di/dt=1A/ns through a 1nH parasitic inductor would introduce a 1V voltage spark. Then how to deal with a processor like Pentium4, in which the di/dt has reached 10A/ns.

Fig.1a shows a simplified power delivery model for Pentium III and Pentium 4 processor. Since we only care about the differential voltage across the decoupling elements, fig.1a is usually further simplified to fig.1b as shown in many literatures. Today’s decoupling approach leads to a lot of bulk caps on the motherboard, and many high frequency caps inside socket cavity, tens of super low ESL cap on OLGA or even specially designed cap inside CPU die which occupying perilous silicon space. The detail of the decoupling design process can be found in [1]~[3].

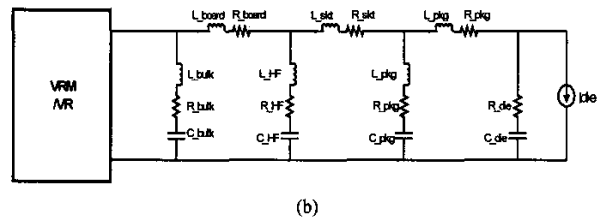
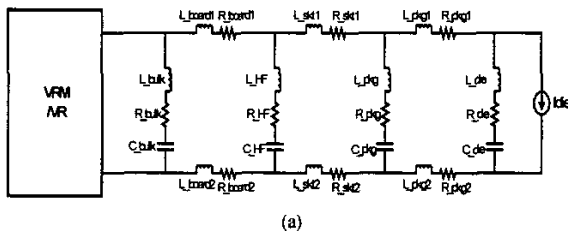
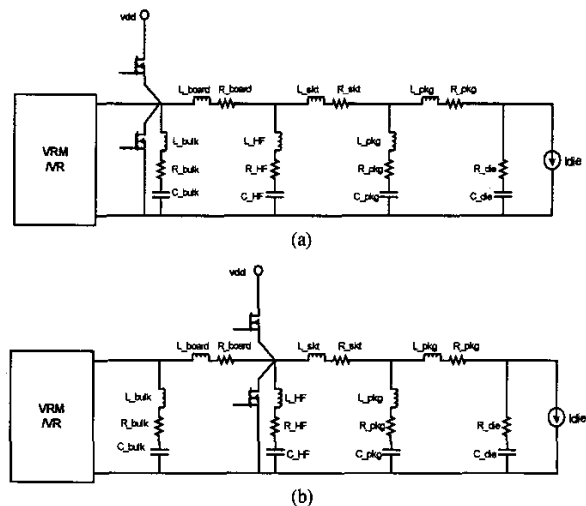


Fig. 1. Power decoupling model of modern microprocessor

However, people are not satisfied with such a space consuming and costly solution. Some prefer to push the VRM switching frequency beyond MHz and using only ceramic caps as bulk caps. [4] The penalty is the significant efficiency reduction of the VRM. Some go even further, push the switching frequency to 4MHz so that VRM can be integrated in microprocessor package. [5] While some more practically, suggest changing part of decoupling caps with active device. There are two ways to use the active devices as decoupling elements. One is “series connection” or “LDO” as in [6]. Another is “shunt connection” or called “Transient Voltage Clamp” as in [7]. As shown in fig.2, intuitively, TVC can be placed on the motherboard to reduce / eliminate bulk cap, or be placed in socket cavity to reduce / eliminate cavity cap, or be placed into CPU package to reduce / eliminate OLGA package cap or/and cap in CPU die.



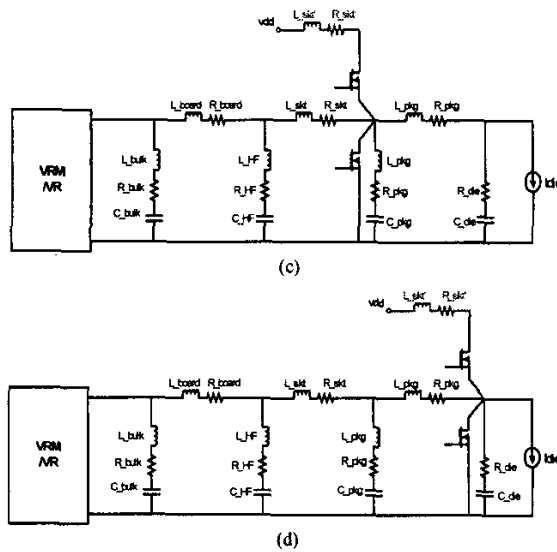
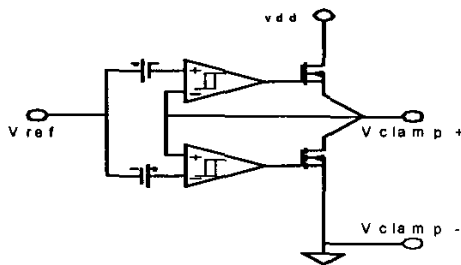


Fig. 2. Possible location of Transient Voltage Clamp (The power devices of TVC can also be BJTs.)

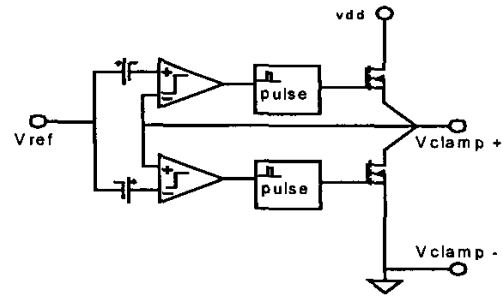
But practically where to put these TVC in the decoupling loop and how to control them is still an open question. This paper will try to discuss these issues. Simulation results of case study will also be given. Section II will answer the control issues of the TVC. Section III discusses where to put the transient clamp. In Section IV, A power management design without Bulk cap on motherboard by using TVC is proposed, which offers Adaptive Voltage Position function and can meet Intel's VRD10.0 [8] specifications. Section V is the conclusion.

II. TVC CONTROL

TVC can be controlled as ON/OFF switches as in fig.3. However the timing to control TVC as an ON/OFF switch is too critical to be practical. Without perfectly tuned hysteretic band and on resistance, it often goes into "oscillation" with the ON/OFF control in fig.3a. As shown in fig 4a, the switches turn on and off at very high frequency for a long time. The ON/OFF Control in fig.3b also has problem. Without perfectly tuned pulse width, the TVC often boost the voltage spike instead of clamping it. fig.4b shows such a case.

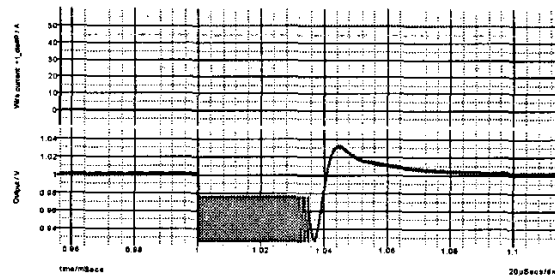


(a) Using hysteretic comparator

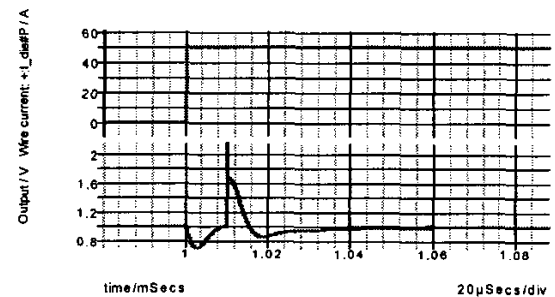


(b) Using pulse generator

Fig. 3. Control TVC as ON/OFF switches



(a)



(b)

Fig. 4. Timing is critical for TVS used as ON/OFF switch (green: load current, red: clamped voltage)

A better way to control the TVC is to make it behave as a bi-directional voltage controlled current source as in fig.5. fig.5a uses the amplifier - power device approach while fig.5b uses monolithic high gain Gm blocks. [9] With the configuration shown in fig.5, the TVC can work smoothly with close-loop controlled VRM. At large transient step, the TVC clamps the voltage across decoupling caps somewhere in the power delivery loop. While at slow transient or steady state, the voltage across decoupling caps is regulated by the close-loop control of the VRM. Therefore, TVC only works at large transient. The system efficiency reduction due to the TVC is limited.

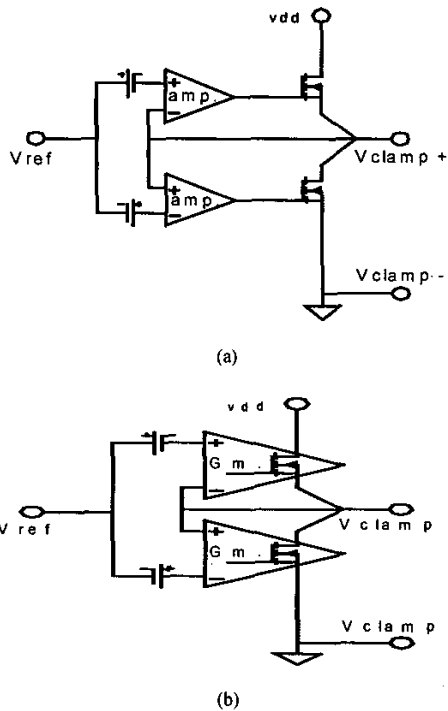


Fig.5. TVC works as a bi-directional voltage controlled current source

III. TVC PLACEMENT

The bandwidth F_b of TVC is not unlimited. To effectively clamp the voltage at different location, the required minimum F_b is different. Our simulation shows that for a CPU with load current transient $di/dt = 10A/ns$, a 10MHZ F_b is needed to clamp the voltage across socket pins, 100MHZ F_b is needed to use TVC to replace caps on the OLGA, 1GHZ is needed to reduce cap inside CPU silicon die.

The slew rate of the current offered from TVC is not only limited by small signal bandwidth, but also limited by parasitic inductance L_s in the TVC loop. To effectively clamp the voltage at different location, the maximum permitted L_s are different. Our simulation shows to clamp the voltage across socket pins, L_s needs to be smaller than 1nH; to use TVC to replace caps on OLGA, L_s needs to be smaller than 10pH; to reduce cap inside CPU silicon die by using TVC, L_s should be smaller than 3 pH. However if we put TVC inside CPU package, a large parasitic inductance due to the socket connection from the outside voltage source to the drain of the “top device” of TVC cannot be avoided. It is in nH range. A remedy to this is put decoupling cap across the “top device”. But that lead to large decoupling cap on OLGA or in the TVC silicon. Our objective of using the TVC to replace the caps cannot be achieved.

Based on the arguments above, the practical place to use

TVC is outside CPU package. A TVC with 10 MHZs bandwidth can be put beside CPU socket to reduce the bulk caps on motherboard or even eliminate the bulk caps.

IV. A VRM-TVC WITHOUT BULK CAP BUT OFFER AVP FUNCTION

Adaptive Voltage Position (AVP) is required by today’s microprocessor power management specification. [8] However no literature reported the TVC application where AVP is necessary. The difficulty to use TVC in AVP case is that the expected output voltage is not a constant.

However, our research indicates that there is a possibility to use TVC while still keeping AVP function. Fig. 7 shows our proposed control scheme. To design a specified load line $R_{droop} = 1.3m\Omega$, the interleaving buck converter working at 500KHZ each phase is used as the power stage. Total inductor current injection control is used to achieve AVP. The V_{ref} added by the current injection signal tells the TVC what is the “right” voltage. The TVC simulated has a $G_m = 1A/mV$. The inductor in each BUCK channel is 200nH. The CPU package parameters used in simulation come from Intel’s documentation. [10] (see fig.6) The only decoupling caps needed on the motherboard are 240uF ceramic caps in the cavity of the socket. There are no bulk caps for this VRM-TVC design. (Tradition VRM approach at the same switching frequency need about 6000uF bulk cap).

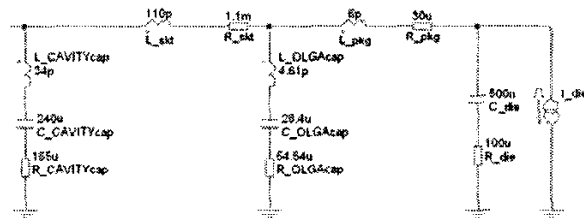


Fig.6. CPU package parameters used in simulation (including cavity caps)

Fig.8 shows the AVP waveforms by using such scheme. The CPU die current change from 0A to 50A with $di/dt = 10A/ns$. The waveforms meet the VRD design requirements [8]. According to the waveform shown in fig.8a, the power loss due to the TVC is below 7W even the full loading-unloading transient repeating at 20KHZ.

As shown in fig.8, proper VRM compensator design is necessary to avoid unnecessary TVC power loss. The TVC supply current to the load only when the V_o is beyond the “steady state window” which is 10mV in our design. While a high voltage loop bandwidth is helpful to leading the V_o into the steady state window. Therefore the objective of the compensator design is to push the voltage loop bandwidth as high as possible. The result is evidential: the design in fig.8a has 3 time bigger voltage loop bandwidth than in fig.8b, which lead to 10 time smaller power loss in TVC power MOSFET.

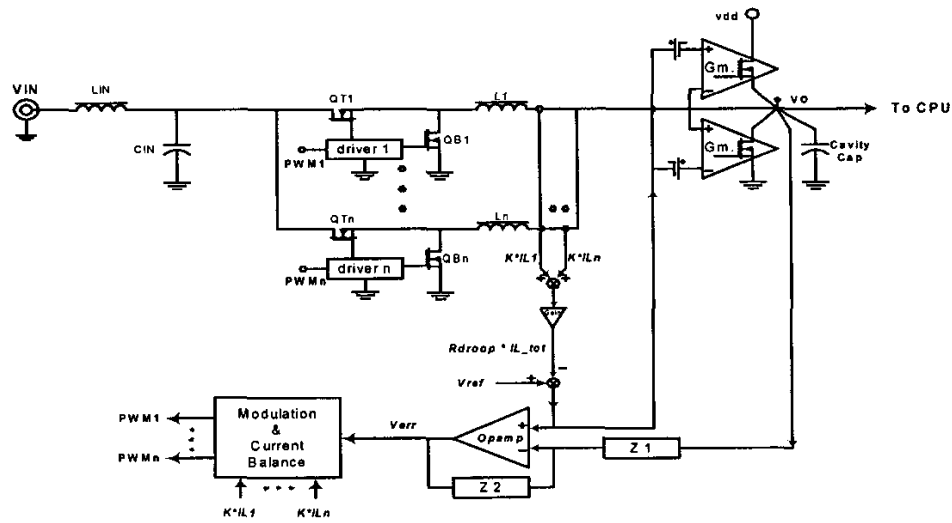


Fig.7. Proposed VRM-TVC design

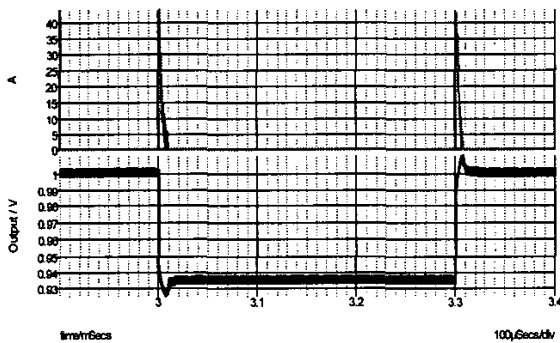
be used in processor power delivery loop design to save system cost or to improve the performance; (2) TVC can be better controlled as a voltage controlled current source instead of an on/off switch; (3) The practical location to use the transient is on the motherboard to save or eliminate bulk caps; (4) The compensator in VRM control loop needs to be carefully designed to avoid unnecessary TVC power loss.

ACKNOWLEDGMENT

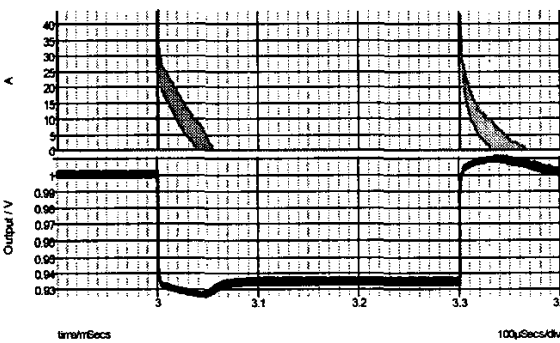
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(a) Low TVC loss with proper VRM compensator design



(b) Large TVC loss due to bad VRM compensator design

Fig.8. Transient waveform of VRM-TVC design with different VRM compensator design (red: current through TVC top device, green: current through TVC bottom device, blue: voltage at CPU socket pins)

V. SUMMARY

Supported by simulation, we can conclude: (1) TVC can