0.35μm, 43 μΩcm^2, 6 mΩ Power MOSFET to Power Future Microprocessor

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Abstract

In this paper, a lateral power MOSFET using 0.35μm VLSI CMOS technology is demonstrated to have a 6 mΩ on resistance and a gate charge of 2.7 nC. For high frequency low voltage power switching conversion applications, the deep sub-micron CMOS/BiCMOS based technology is clear superior to conventional vertical power MOSFET technology.

Introduction

With the increasing speed of the microprocessor, and its demand for far more power, how to power the microprocessor of our computers becomes an important issue. The requirement of the Voltage Regulator Module (VRM) for the future generations of microprocessors can be summarized as: (1) Low output voltages (1.0-1.8V), (2) High load current (30-70A, and possibly more), (3) Faster transient response with a current slew rate higher than 5A/ns, (4) High power density. So far, none of the conventional VRM can meet all of the four requirements while maintaining acceptable power conversion efficiency. One possible solution is the interleaved quasi-square-wave (QSW) converter working at multi-megahertz [1]. As a consequence, the power switches used in the future VRM's have to be able to work efficiently at higher switch frequency and with higher current density. While the voltage blocking capability is no longer a major issue, the main emphasis shifts to the trade-off between the conduction loss and the switching plus gate-drive losses. A good way to judge the efficiency performance of the power MOSFET is to compare the figure of merit (FOM) defined as [2]

$$\mathrm{FOM} = R_{on} \cdot (Q_g + Q_{gs} + Q_{th} + Q_{gd}) \qquad (1)$$

where Qg, Qgs, Qth, and Qgd are defined in Figure 1.

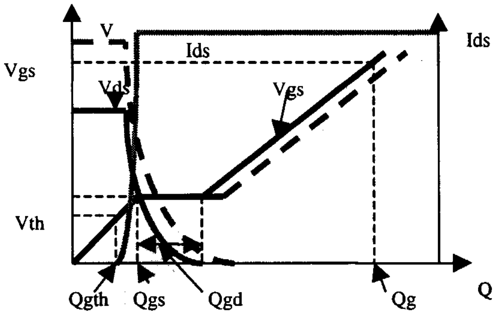

Figure 1. Typical gate charge wave form of a power MOSFET.

As shown in Table 1, the smaller the FOM, the better the device in terms of the ceiling efficiency, which is the maximum efficiency as shown in Figure 2 and 3. The ceiling efficiency for a given power MOSFET technology, or a given FOM, is reached when the conduction loss is equal to the sum of switching loss and gate drive loss.

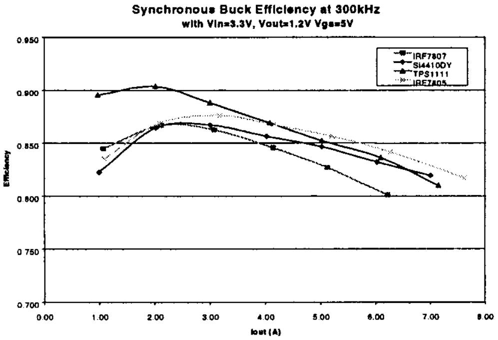

Figure 2. Synchronous buck converter efficiency at 300 kHz.

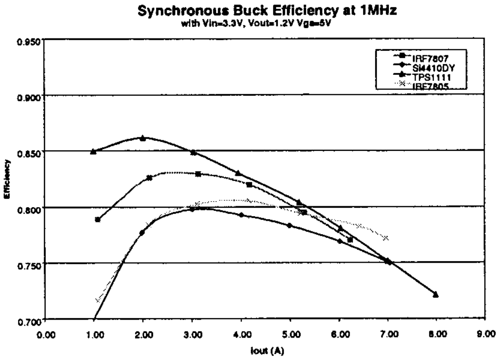

Figure 3. Synchronous buck converter efficiency at 1 MHz

Impact of Voltage Scaling on Vertical MOSFET

Extensive experimental test results as shown in Figure 2 and Figure 3 are strongly in favor of lateral power MOSFET over vertical power MOSFET. However the voltage rating is also in favor of the TPS1111N's 7V compared to the others of 30V. Will lowered voltage rating help the performance of VDMOS? Our extensive MEDICI simulation results show that once the voltage rating gets into sub 20V range, the improvement for the vertical power MOSFETs in terms of the FOM as defined in (1) is very little. Figure 4 shows the half gate length optimization in terms of the specific on-resistance for VDMOS with a gate oxide thickness of 25 nm. As shown in Figure 5, the gate charge Qg will increase monotonically as the half-gate length increases. The optimized half-gate length is also different for minimum FOM (shown in Figure 6) as compared for minimum specific on-resistance. Two aspects remain to be the major barriers of the voltage scaling down in the VDMOS. One is the 90 μΩ cm^2 of specific resistance due to the substrate, which exists in all vertical power devices. The other is the parasitic JFET effect, which limits the channel density increase for the VDMOS.

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Table 1 FOM and Ceiling efficiency comparison for current and future devices used in synchronous buck converter

Vin=3.3V Vout=1.2V Vgs=5V	Ron *(mΩ)*	Qg (nC)	FOM *(mΩ* nC)*	Ceiling Efficiency (%)			Technology
				300 kHz	500 kHz	1 MHz	
Si4410DY (30V, 10A) (i)	16.5	25	566	86.7	83.0	79.0	Trench MOSFET from Temic Corp.
IRF7805 (30V, 13A) (ii)	10	29	389	86.9	85.6	80.0	Conventional VDMOS from International Rectifier, Inc.
IRF7807 (30V, 8.3A) (ii)	20	14	368	87.6	85.7	82.9	Conventional VDMOS from International Rectifier, Inc.
TPS1111 (7V, 12A) (iii)	21	7.7	**183**	90.4	89.3	86.1	N channel LDD MOSFET from Texas Instrument, Inc.

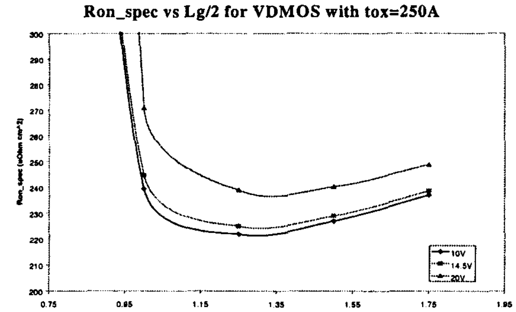

Figure 4. Impact of half-gate length on specific on-resistances for VDMOS. The JFET effect and the 90 μΩ cm^2 of specific resistance due to substrate (already included) are two major barriers for VDMOS voltage scaling.

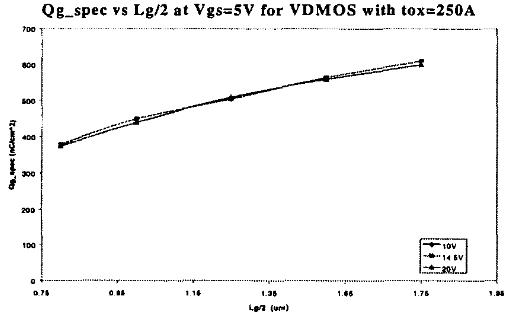

Figure 5. Impact of half-gate length on specific gate charge for VDMOS.

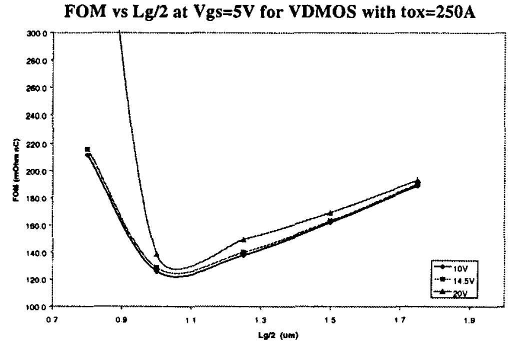

Figure 6. Impact of half-gate length on FOM for VDMOS

LDD MOSFET-A Better Solution

One alternative device that eliminates both the substrate resistance and the JFET effect is the LDD MOSFET, as shown in Figure 7 [2]. For a meaningful comparison, a gate-length of 0.4 μm is used, and the gate oxide thickness is chosen to be 25nm, which is the same as that of the VDMOS discussed previously. Some concerns, however, have been shown in the past with respect to the metal trace de-biasing effect in lateral devices. [3] [4] Care must be taken in terms of layout design. One way to minimize the de-biasing effect is to use three metal layers instead of the two as shown in Figure 8.

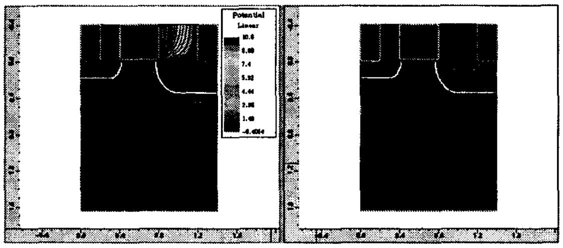

Figure 7. Equal-potential contours of the 10 V LDD MOSFET, at the breakdown, Vgs=0V, Vds=10V (left) and current flow lines in the on-state, Vgs=5V, Vds=0.1V (right)

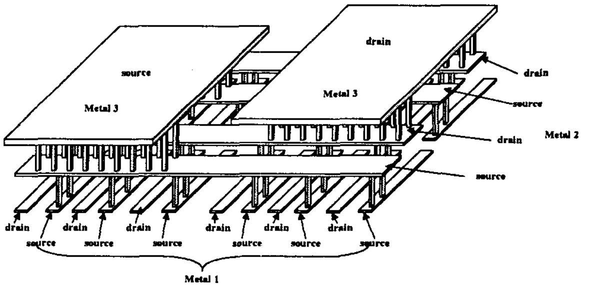

Figure 8. The conceptual layout using three metal layers.

A useful model to estimate the de-biasing effect is a pure resistance network as shown in Figure 9.

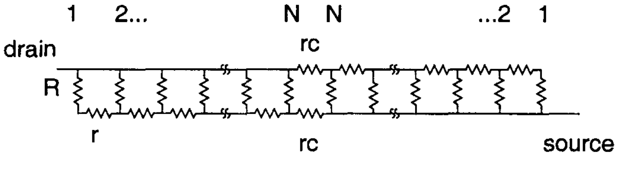

Figure 9. Resistance network used to calculate the de-biasing effect
R = $R_{on\_sim}+R_{contact}$, r = resistance of metal trace between two unit cell,
rc = resistance of metal trace between drain pad and source pad.

Its equivalent resistance can be calculated by the asymptotic formula shown in the Equation (2).

$$R_{eff} = \frac{\sqrt{rR}\coth\left(\sqrt{\frac{r}{R}}N\right) + rc}{2} \qquad (2)$$

Calculated results of resistance with different die sizes are shown in Table 2. A sheet resistance of 0.06 Ω per square is assumed for all three metal layers.

Table 2. 10V LDDMOS resistance evolution with die size change

Die Size	N	R (Ω)	r (Ω)	rc (Ω)	R_{eff} (Ω)	R_{spec} (μΩ cm^2)
1.4μm x 1.6 μm	1	2691			2691	60.28
1.4 μm x 329.6 μm	100	2691	0.24	0.72	17.36	80.1
329.6 μm x 942 μm	330	17.36	5.25 x 10^{-4}	2.2 x 10^{-3}	0.0514	159.6
1mm x 5 mm	14	0.0514	0	0	0.0037	185
1mm x 10 mm	28	0.0514	0	0	0.00185	185
2 mm x 5 mm					0.0035	350

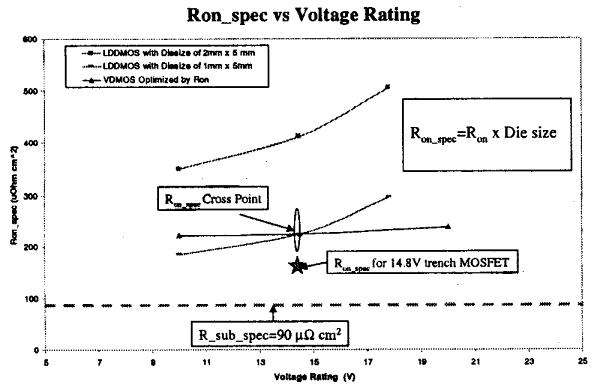

Figure 10. Specific on-resistance comparison, excluding resistances due to wire bonding and packaging

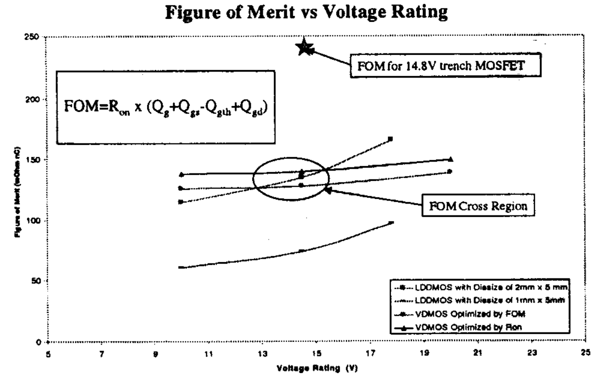

Figure 11. FOM comparison, excluding resistances due to wire bonding and packaging

Even with the consideration of metal trace de-biasing effect, for sub 20V applications, the lateral structure still has its advantages over vertical structure in terms of gate charge and Miller capacitance. This is especially important for high frequency applications. From Figures 10 and 11, one can see that there exists a voltage crossing point, below which the lateral structure shows its full advantages in both specific on resistance, gate charge and Miller capacitance.

VLSI CMOS Realization and Device Performance

By using, MOSIS HP-0.35 μm VLSI CMOS process, we have made three lateral MOSFETs with varied gate length design on a 2 mm by 2 mm chip (Figure 12).

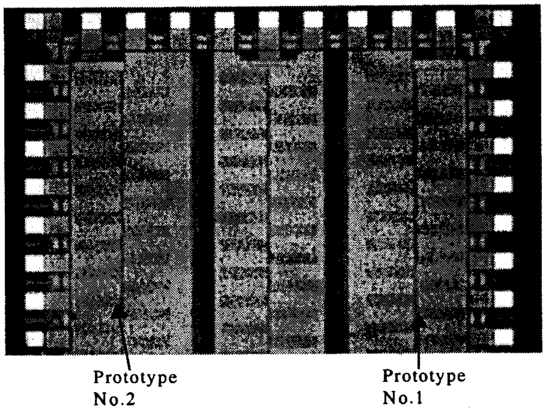

Figure 12.Top view of our prototype lateral NMOSFET using MOSIS HP 0.35 μm CMOS process with three metal layers

Two of them have proved to work very well. Figure 13 and Figure 14 show the gate charge at different gate voltage of the two devices respectively. Figure 15 and Figure 16 show the on state I-V curve using four-probe test method.

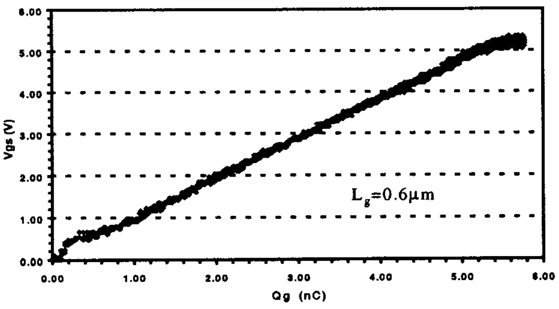

Figure 13. Gate charge wave-form for Prototype No.1. Lg(draw)=0.6μm.

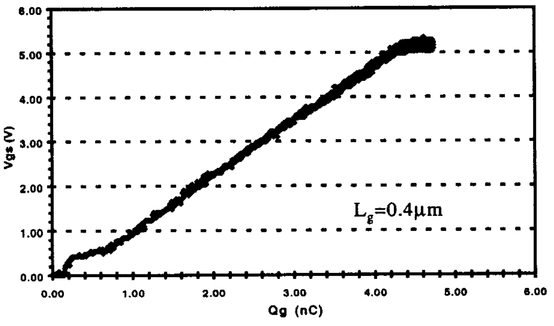

Figure 14. Gate charge wave-form for Prototype No.2. Lg(draw)=0.4μm.

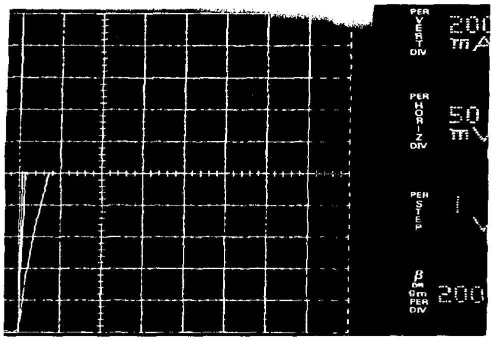

Figure 15. Ids v.s. Vds at Vgs=1V, 2V, and 3V, No.1. Lg(draw)=0.6μm.

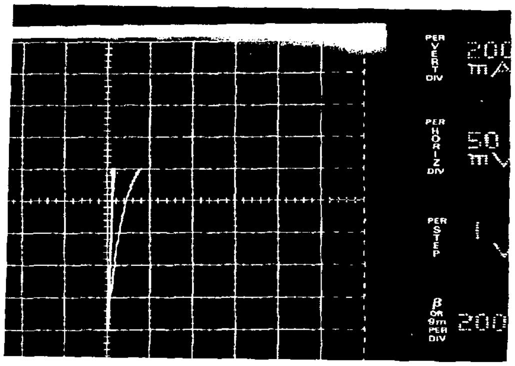

Figure 16. Ids v.s. Vds at Vgs=1V, 2V, and 3V, (No.2. Lg(draw)=0.4μm.)

From Figure 15 and Figure 16, we can see that both devices have a very low on resistance (excluding the packaging resistance), which is about 6 mΩ at V_{gs}=3V and I_{ds}=1A. Figure 17 and Figure 18 show that both devices have the similar breakdown voltage of about 7.4V at a leakage current of 10μA. However, if compare Figure 13 and Figure 14, we can see that Prototype No.2 has less gate charge, of about 2.7nC at Vgs=3V, against the 3.2nC of prototype No. 1 at the same gate voltage. Therefore, in terms of FOM defined earlier, prototype No 2 with drawing gate length of 0.4μm is better.

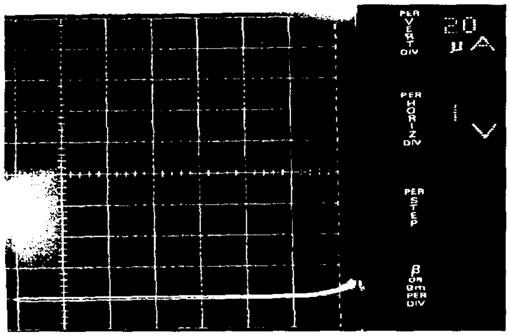

Figure 17. Ids v.s. Vds at Vgs=0V, the breakdown voltage is about 7.4V at Ids=10μA (No.1. Lg(draw)=0.6μm.)

Table 3 summarizes several important electrical parameters of the two power MOSFETs. It is worthwhile to point out that in terms of FOM, prototype No. 2 (7.4V break down) is about 1/10 of that of TPS1111N (best industrial prototype available) and about 1/20 of that of the best commercial power MOSFET.

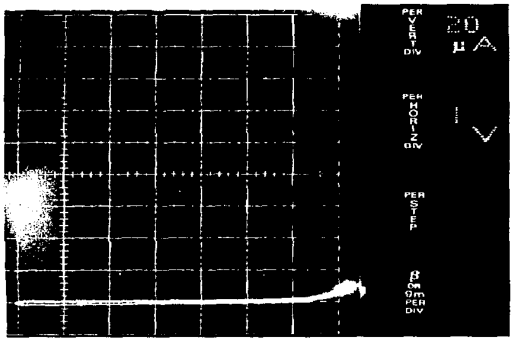

Figure 18. Ids v.s. Vds at Vgs=0V, the breakdown voltage is about 7.4V at Ids=10μA (No.2. Lg(draw)=0.4μm.)

Table 3. Major electrical parameters of our n channel lateral MOSFET fabricated by MOSIS HP 0.35 μm process

	Prototype No. 1	**Prototype No. 2**
Lg (μm)	0.6	0.4
BV (V)	7.4 at 10μA	7.4 at 10μA
Vth (V)	0.62	0.55
Active Area	1.6mm x 0.445mm	1.6mm x 0.45mm
Ron (mΩ) at Vgs=3V	6	6
Ron_spec at Vgs=3V	43 μΩ cm^2	**43 μΩ cm^2**
Qg (nC)	3.2	**2.7**
Qgd (nC)	0.37	0.4
Qgs (nC)	0.12	0.12
Qgth (nC)	0.115	0.113
Ciss (pf) (max)	559.7	487.3
Coss (pf) (max)	385.3	425.5
Crss (pf) (max)	126.6	168.5
FOM (mΩ nC)	21.45	**18.63**
Body Diode Forward Voltage (V)	0.6	0.6

Conclusion

We have successfully demonstrated a 7V Power MOSFET using sub-micron VLSI CMOS technology. Our test results show that this lateral MOSFET has advantages over conventional vertical MOSFET on both specific on resistance and gate charge. It also demonstrates the feasibility of integrating future VRM monolithically with other digital control and gate drive circuits.

Acknowledgement

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