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Low Voltage Power Devices for Future VRM

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Abstract

In this paper, a fully depleted LDD MOSFET built on Silicon-on-Oxide is proposed as a candidate device for future VRM, which is expected to work at multi megahertz.

Introduction

Voltage Regulator Module (VRM) is a dedicated DC/DC converter to power advanced microprocessors such as the Pentium processor from Intel. Future generation microprocessors are expected to operate at a much lower voltage of about 1 V instead of today's 3.3 V, with a much heavier load in the range of 30-70A and a much faster transient slew rate of 8 A/ns. Future VRMs will also have a very tight voltage tolerance (e.g. 2% for 1.1 V VRM output, and the voltage deviation can only be ± 33 mV). These requirements pose serious design challenges. Table 1 shows the specifications for current and future VRMs. Three issues have to be addressed to meet the requirement of future VRM. These are 1) VRM topology; 2) system integration and 3) low voltage power devices.

Except for adding capacitors, it is difficult for conventional VRMs to meet the transient requirement [1]. With interleaved quasi-square wave (QSW) topology, the transient response can be significantly improved without increasing capacitor numbers [2]. By increasing the switching frequency to multi-megahertz, the output inductance can be significantly reduced, so is the de-coupling capacitance, while the transient performance is further improved. All these lead to a possibility of integrating future VRM with the microprocessor. It can be fulfilled by either a hybrid approach or monolithic approach. In the hybrid approach, VRM integrates together the control unit, the gate drive circuit and the power switching devices, and the VRM is then mounted on the same cartridge of the processor. In the monolithic approach, the VRM is integrated together with the microprocessor in one chip and operated at multi-megahertz frequency. However, none of today's power devices can provide an acceptable power conversion efficiency at multi megahertz due its poor conduction loss and switching plus gate drive loss trade off. Besides, the traditional VDMOS technology is also not suitable for hybrid or monolithic integration. These all indicate that the power device technology for future VRM belongs to a VLSI compatible technology, and high speed (low gate charge, no Miller capacitance) is more important than just low on-resistance.

Table 1 Requirements of current and future VRMs

	Current	Future
Output voltage	2.1-3.5 V	1.0 - 2.2 V
Load current	0.3 - 13 A	1 - 50 A
Output voltage tolerance	± 5%	± 2%
Current slew rate	1A /ns	8 A/ns

Current Status of Low Voltage Power Devices

Today's low voltage power devices are commercially available at a rating of around 30V based on vertical power MOSFET technology. However, future VRM requires power devices with the following characteristics: 1) lower breakdown voltage (< 10V); 2) lower $R_{on} \times Q_g$ product; 3) lower Miller capacitance.

Device Figure of Merit for High Frequency Application

The total power loss of a power device under high frequency operation can be categorized into three parts. (1) The conduction loss, which is proportional to Ron, therefore is inversely proportional to the die size. (2) The gate drive loss, which is proportional to total gate charge, therefore is proportional to the die size. (3) The switching loss, which increases as the rising and falling time increase (which are determined by Q_{gs}-Q_{th}+Q_{gd}), is also roughly proportional to the die size. For simplicity and generality, we can define the following device figure of merit

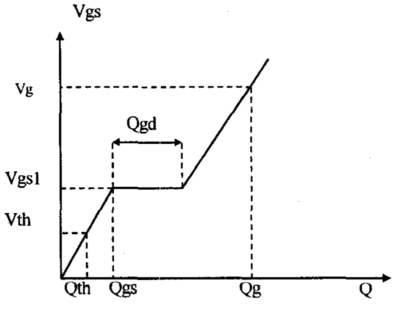

Figure 1. Typical gate charge waveform

(FOM) based on efficiency consideration.

$$FOM=R_{on}\times (Qg+Q_{gs}-Q_{th}+Q_{gd}) \tag{1}$$

Where R_{on} is the on-resistance, while Q_g, Q_{gs}, Q_{th} and Q_{gd} are defined in Figure 1.

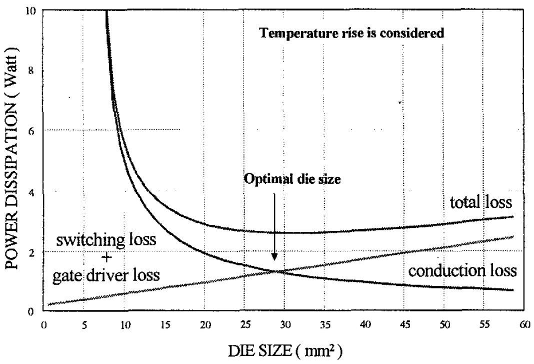

Figure 2. Trade-off between conduction and switching plus gate loss of a power MOSFET for a given FOM.

Figure 2 shows the basic trade-off of a commercial power MOSFET IRF3803 between its conduction loss and switching plus gate loss. The maximum or ceiling efficiency is reached when the conduction loss equals to the switching plus gate losses for a given condition. In Table 2, synchronous buck converter efficiency is shown based on the method proposed by Spaziani [3] for several commercial devices. Table 2 indicates a strong relationship between the FOM and the efficiency of the converter. The smaller the FOM, the better the performance of the device in terms of efficiency.

Table 2 FOM and Ceiling efficiency comparison for current and future devices used in synchronous buck converter

Vin=3V Vout=1.5V	FOM *(mΩ* nC)*	Ceiling Efficiency (%)		
		300kHz	700kHz	1MHz
IRL3102 **	981	87.6	78.6	73.4
IRL3302 **	821	90.0	82.7	78.2
SUD50N03-10 *	761	90.1	83.3	78.9
Si4410DY *	750	90.9	84.1	79.9
Si4466DY *	585	92.2	86.0	86.0
Best VDMOS #	216	94.1	90.4	88.2
LDDMOS-SOI #	82	95.5	93.3	92.0

**: Conventional VDMOS technology
*: Trench MOSFET
#: Simulation result, assuming 0.25 um technology

Impact of VLSI Technology on Conventional VDMOS Design

In today's state-of-art VDMOS technology, the design rules used are still in the micron order, unlike the sub-micron and even deep sub-micron technology which are widely used in the VLSI area. The impacts of sub-micron or deep sub-micron technology on the VDMOS are shown in Figure 3 to Figure 6 based on extensive MEDICI simulation. Results show that there are still rooms for improvement when the voltage rating as well as the ploy opening is scaled down. The simulation result predicts that the best VDMOS will improve the FOM by a factor of 3-4 as shown in Table 2, assuming that a quarter micron technology is employed for the VDMOS. The main reason is that the voltage rating and design rule scaling down will help to increase the channel density, therefore, decrease the overall specific on-resistance. However, as shown in Figure 4, 5 and 6, the inherent JFET effect and the resistance of the thick N^+ substrate will prohibit its further scaling. Besides, the relatively large gate charge and Miller effect will limit its application in multi-megahertz application such as the future VRM. As result, one should look for other device structures that provide a better trade-off between the on-resistance and the gate and Miller charges.

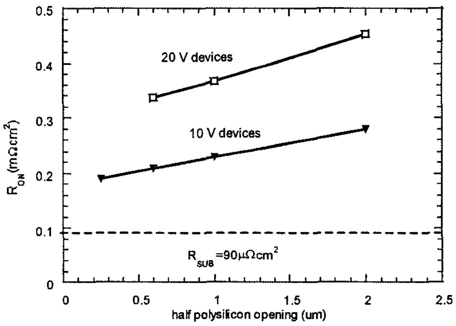

Figure 3. Impact of VLSI design rule on VDMOS performance, showing the substrate resistance limitation

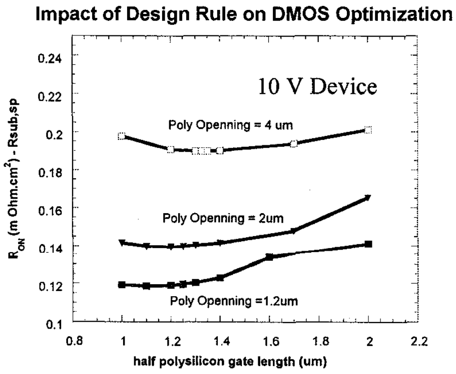

Figure 4 Impact of VLSI design rule on DMOS performance, showing the JFET limitation.

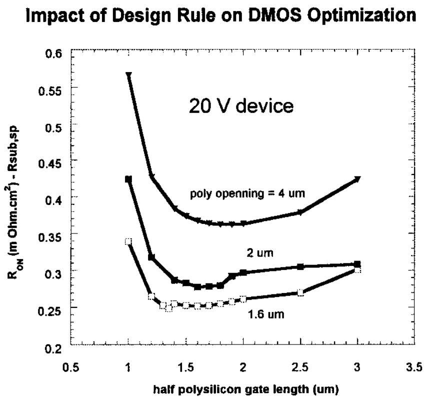

Figure 5 Impact of VLSI design rule on DMOS performance, showing the JFET limitation.

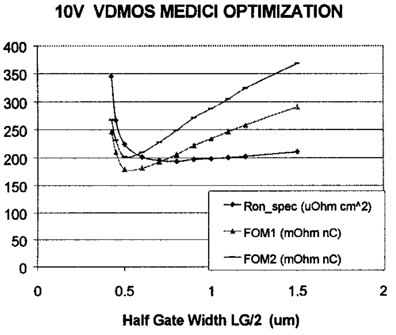

Figure 6. Impact of VLSI design rule on VDMOS optimization. Where
FOM1=Ron*Qg
FOM2=Ron*(Qg+Qgs-Qth+Qgd)

Future Low Voltage Power Devices

Apart from further scaling down the design rule for conventional VDMOS technology, many efforts have been made in the development of trench technology. From Table 2, it is clear that the trench devices do have a better performance over traditional VDMOS devices because the JFET effect has been greatly reduced. However, the substrate resistance still exists in the trench technology, which is still a major barrier for further performance improvement.

Further improvement of the FOM in sub-20-V devices can be made by using the high-speed VLSI technology [4][5][6]. The best-suited device structure, based on our simulation, is a fully depleted lateral Lightly Doped Drain (LDD) MOSFET built on a thin Silicon-on-Insulator (SOI). Based on extensive numerical simulations (e.g Figures 8 and 9), it is concluded that the fully depleted LDD MOSFET on SOI (shown in Figure 7) provides the best FOM when advanced VLSI design rule is used.

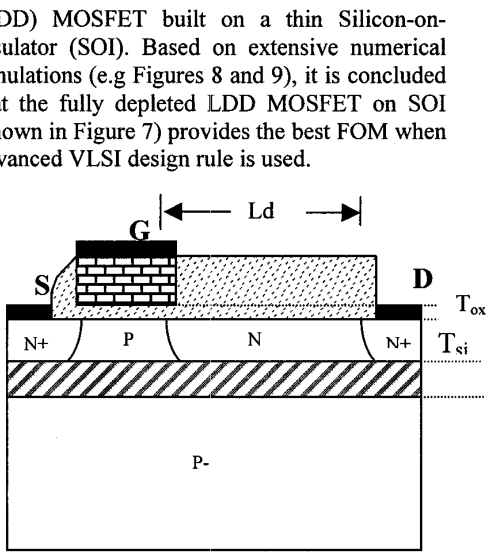

Figure 7 SOI LDD MOSFET provides possibility of very low Ron x Qg product and is capable of monolithic integration with CPU

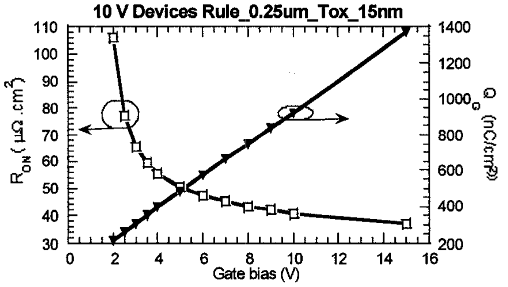

Figure 8. Effect of gate bias on Ron and Qg optimization.

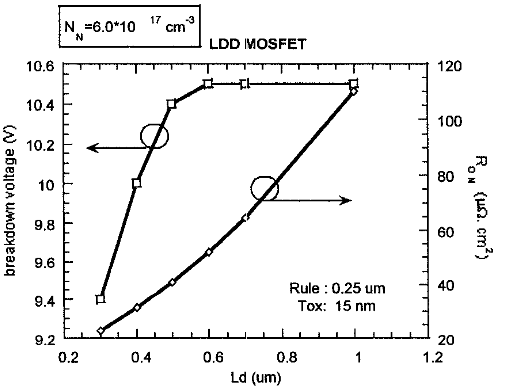

Figure 9. Effect of Ld length on blocking capability and Ron

Table 3 Efficiency comparison in interleaved multi-channel QSW VRM [2]

Vin=5V, Vout=2V	Rule//Tox	BV (V)	Ron (mΩ)	Qg (nC)	Qgs (nC)	Qth (nC)	Qgd (nC)	FOM (mΩnC) **	Optimized Efficiency * for Interleaved QSW VRM		
									300kHz 16 Modular	1MHz 16 Modular	10MHz 48 Modular
LDDMOS	**0.25um/15nm**	**10**	**0.97**	**77**	**2**	**1.8**	**7.9**	**82.8**	**95.2%**	**91.2**	**88.5%**
Best VDMOS	0.25um/10nm	16	2.4	80	7.0	4.5	8	216	93.6%	87%	75.9%
Typical Value for Current Device	N/A	30	10	60	10	5	10	750	87%	79%	60%

*With the integration approach, the VRM layout loss is minimized
**FOM=Ron*(Qg+Qgs-Qth+Qgd)

The results in Table 2 shows a factor of 3 improvement in terms of FOM when LDD MOSFET on SOI is compared with the projected best VDMOS, and a fact of 7 improvement when compared with the best trench device. Most important of all, however, is that the compatibility with standard Bi-CMOS technology makes the SOI LDD MOSFET even more attractive when further integration with control units and gate drive circuits are needed. Monolithic integration of the LDD MOSFET with a BiCMOS process based processor is also possible.

Table 3 shows the simulated efficiency comparison of a multi-channel interleaved QSW VRM, which naturally cancels the output current ripple and still keeps the fast transient response characteristics of the QSW topology. As the switching frequency increases to multi megahertz range, the de-coupling capacitance can be significantly decreased and the magnetic core can be essentially eliminated in the VRM [2]. From Table 3, it is clear that the efficiency of the LDD MOSFET based QSW VRM is still higher than 88% even when it operates at 10 MHz. Furthermore, by reducing and eliminating the interconnection trace, one can further lower the power loss due to the trace resistance, and decrease the transient spikes due to the interconnect inductance. All these make the integration even more necessary. Devices such as the SOI LDD MOSFET certainly will make that a possibility possible.

Conclusion

The fully depleted SOI LDD MOSFET substantially has (1) very low Miller capacitance and gate capacitance; (2) higher channel density, therefore very low specific on-resistance; (3) compatibility with VLSI Bi-CMOS technology.
It is highly suited in high switching frequency, high current load, low voltage power conversion applications such as the future VRM.

Acknowledgement

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