

Design of a monolithic high frequency fast transient buck for portable application

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Abstract— The earth is mobile. There is a huge market for mobile power management ICs today and in the future^[1]. Fast transient response, efficient performance, small profile and low cost are the most desired features for mobile power management IC. In this paper, a 2MHz high efficiency, wide input range monolithic buck DC-DC converter ASIC is designed based on advanced trench BCD process. Some important design issues such as compensator design for wide range of input, output voltage and load current, linear-non-linear control for fast transient response, efficiency optimisation, device optimisation, noise separation and driver design are discussed. The experiment test results show that the ASIC works well.

I. INTRODUCTION

The earth is mobile. There is a huge market for mobile power management ICs today and in the future^[1]. Fast transient response, efficient performance, small profile and low cost are the most desired features for mobile power management IC. In order to reduce profile, the number of external components should be as small as possible, which means that we need to integrate compensator, external ramp, current sensor, driver and power devices all in a single chip, i.e. monolithic integration. Future development will even make it possible to integrate the energy storage elements, such as the inductor and capacitor. This development relies on further technology development in the area of high-density inductor and capacitor design that is compatible with semiconductor technology, as well as the techniques to operate the converter at extremely high frequencies, such as 100 MHz^{[2][3]}. Comparing with discrete switching DC-DC converter, monolithic integration brings a number of benefits and new challenges: The number of external components can be reduced to only the main inductor and output capacitor so the power density can be increased drastically; The parasitic components such as bond wire inductance, trace resistance are reduced, which is important for high frequency and noise sensitive applications^[4]; Since compensator, ramp compensation and current sensor are integrated inside chip, how to design the compensator to stabilize the system for wide input and output ranges is a big challenge. Since power devices and drivers are integrated with control circuit, noise can be easily injected from power stage to analog control part. How to provide noise separation between power stage and control part is an issue

for monolithic integration; Since the battery source for portable power can be a single 1.2V nickel metal hydride with a final discharge voltage of 0.8V to several 4.3V Lilon batteries in series^[1], both low-voltage and high-voltage operation may be required for portable power ICs. At the low-voltage end, low-voltage analog IC design is a challenge. At the high-voltage end, higher-voltage CMOS or CMOS variants are needed for high-input-voltage applications.

Besides monolithic integration, high switching frequency is another trend for portable power management IC due to its higher bandwidth and its ability to further reduce external passive component size. In this paper, a 2MHz high efficiency, wide input range (3-24V) monolithic buck DC-DC converter ASIC is designed based on advanced trench BCD process.

II. CHIP DESIGN CONSIDERATION

Fig. 1 is the simplified block diagram of the ASIC chip. The main control loop uses peak current control in parallel with a novel non-linear control. We call it "linear-non-linear" control^[5]. Two 30V N channel LDMOS are used as top and bottom switch. Two current sensors are included for both top and bottom switches. Under voltage lock out, over voltage protection, over temperature protection and output short circuit protection are designed for robustness. In the following sections, some critical design issues will be discussed.

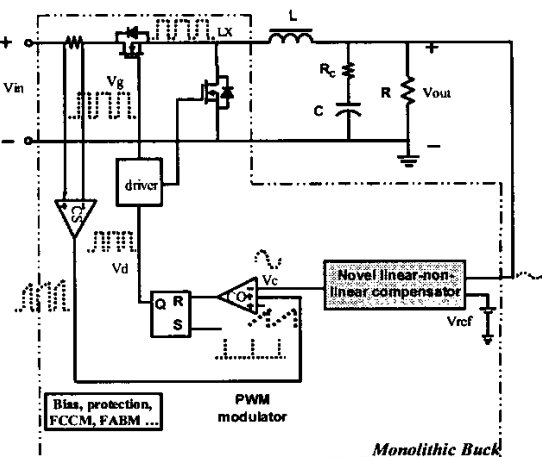


Fig. 1 Simplified functional block diagram

A. Novel linear-non-linear control for fast transient response

Fast transient response is an important requirement for most of the DC-DC converters, especially for portable application since the output voltage is going lower and lower and the tolerance is smaller and smaller. For a traditional linear peak current control, the rising speed of inductor current during the step up transient period is strongly limited by the bandwidth of the control loop and slew rate of the error amplifier. A large voltage drop will happen at the output voltage. For step down transient, a voltage spike can happen at the output voltage too for the same reason. At another extreme case, if a bang-bang control is used to saturate the duty cycle during transient period, a stability problem can happen for some case and the inductor current may oscillate. In this chip, a novel "linear-non-linear" compensator is proposed to speed up the transient response. In steady state, the non-linear control loop will not be in action so that the output voltage is mainly maintained by the linear peak current control loop. The chip operates as a normal peak current controlled system with a small output ripple. When the load current steps up or steps down, the non-linear loop will be activated and speeds up the voltage recovery process. Fig.2 shows the corresponding system loop gain during transient period. From Fig.2, one can see that during transient period, the bandwidth of the system loop gain is much higher than original peak current loop. So the output voltage can be recovered quickly. Since loop gain is a steady state concept, it may not accurate to model loop gain during transient period. However, the recover period is much shorter than the traditional peak current control. Fig. 3 is the transient response results with and without "linear-non-linear compensator". With "linear-non-linear compensator", the inductor current can change to the new steady value quickly to reduce the voltage error. The voltage drop with non-linear control at step up transient period is only 1/3 of the voltage drop without non-linear control. The same result is shown in step down transient period. This is very important for low voltage portable application.

Fig. 2. System open loop gain with nonlinear control during transient time

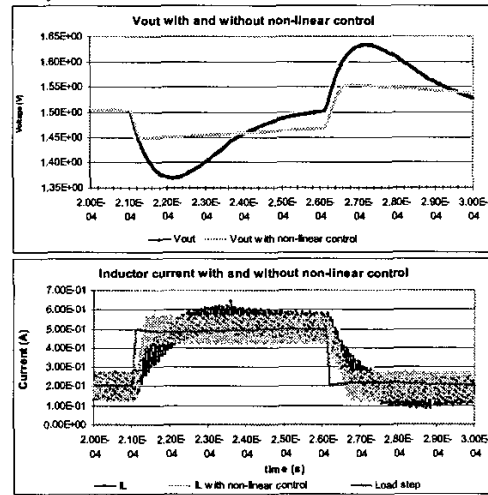


Fig. 3. Transient response with and without non-linear control

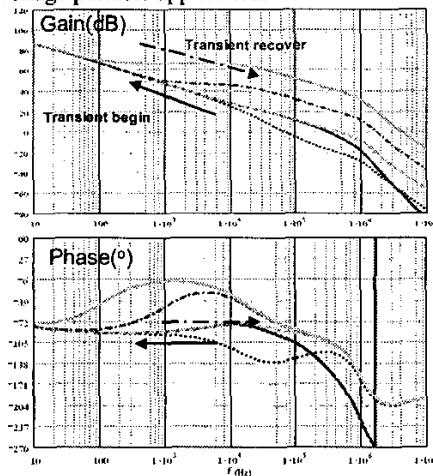
B. Stability modelling and loop design for wide application range

One chip for multi markets is a normal case in industry now. The input voltage, output voltage, load current and even switching for the same chip in different applications may be quite different. Since compensator, ramp compensation and current sensor are integrated inside the chip, the end user cannot change the compensation to fit a specific application. How to design a fixed compensator to stabilize the system for wide input and output ranges is a big challenge. According to [6], when the current loop is closed, the power stage is degraded to a one-order system. The compensation is designed based on the transfer function G_{oc} from V_c to V_{out} . For different applications, the dominant pole ω_{pdom} of G_{oc} are moving with duty cycle D and load current as shown in equation (1).

$$\omega_{pdom} \cong \frac{1}{R \cdot C} + \frac{T_s}{L \cdot C} \cdot (m_c \cdot D' - 0.5) \quad (1)$$

R is the load resistance, C is the output capacitor, L is the main inductor, T_s is switching period, m_c is the ratio of inductor current slope and ramp compensation slope, D' is $1-D$ (D is duty cycle)

In order to make the system loop stable for different applications, adaptive compensation concept is proposed, which means that the zero in the compensator will move to low frequency when load current increases. Design is made based on the worst-case operation situation. All of the working conditions are then evaluated to guarantee the stability for all operation ranges. A saw tooth signal shown in Fig. 1 is used for slope compensation when duty cycle is larger than 50%. Although it is quite difficult to make the single pole of control-to-output transfer function with current loop closed to be equal to the compensation zero when input, output voltage, load current and even switching frequency change, the test results show that the designed chip works well over a wide operation ranges.



C. High efficiency design

High efficiency is another important factor for portable power management ASIC since most of portable applications are powered by mobile energy source such as batteries. In order to keep high efficiency at the whole load current range, a multi-section LDMOS device structure is used in this ASIC. During light load, only 1/3 of the device is used. So the gate charge loss and switching loss are reduced. Comparing with single-section device, efficiency can be improved by one to two percents at light load. When the load is very small like 1mA, traditional peak current control converter will work in discontinuous current mode (DCM) and keeps turning the switches on and off. The power loss of the control core and driver are unbearable comparing with the small load. In this chip, three different work modes are used to further improve light load efficiency: Frequency Adjustable Burst Mode (FABM), DCM mode and Forced Continuous Current Mode (FCCM). FABM is a high efficiency mode. The frequency can be adjusted to a certain frequency so the switching noise can be filtered out by system filter. FCCM is for noise sensitive application such as RF application. The inductor current in this mode is continuous so less noise will be generated.

D. Power device design

TABLE I
Main parameters for power devices

Parameters	Bottom NMOS	Top NMOS
W (cm)	2.325	1.55
L (um)	0.5	0.5
R_{dson} (mΩ)	150	240
Q_g ($ V_{gs} =5V$) nC	1.85	1.234
Q_{gs} ($ V_{gs} =1.22V$) nC	0.068	0.0467
Q_{gth} ($ V_{gs} =1V$) nC	0.052	0.034
Q_{gd} ($ V_{ds} =5$ to $0V$) nC	0.426	0.286
Figure of Merit ^[9] = R_{dson}^* ($Q_g+Q_{gd}+Q_{gs}-Q_{gth}$)	343.8 nCmΩ	367.8 nCmΩ

Two 30V power NLD MOS are integrated in this chip as top and bottom power switches. Fig. 4 is the cross-section of the LDMOS [7]. The optimization of the device size is based on the switching loss and conduction loss. Since this chip is used mostly at low duty cycle applications, conduction loss is dominant for bottom switch and switching loss is dominant for top switch. A larger device is chosen as the bottom switch to reduce conduction loss. Table I lists the main electrical parameters for these two devices. One can see that, since C_{gd} is much larger than C_{gs} , a long holding period will be generated during switching and the switching loss will increase.

Fig. 5 (a) shows the parasitic capacitance and $R_{ds(on)}$ simulation by ISE software [8]. Fig. 5 (b) is the breakdown simulation by ISE software. The breakdown point happens at the bird's beak of the field oxide. In [7], the effect of different layout structure on the hot carrier and SOA is

discussed. In this chip, a chessboard drain ring array structure is used for both top and bottom switches. Fig. 6 (a) shows the needed SOA for top switch generated by system level simulation including packaging parasitic components. Fig. 6(b) is the needed SOA for bottom switch. It is clear that the required SOA for top switch is much larger than the bottom switch. Select a large SOA device is therefore important to ensure reliable operation. Fig. 6(c) shows the measured SOA for the LDMOS using different layout structure [7]. One can see that, the needed SOA is within the measured SOA. As a matter of fact, the LDMOS SOA is too large for this application hence further improvement is possible by reducing the SOA. This will result in improved FOM value [9]. Fig. 7 shows the loss breakdown for switching frequency at 1.5MHz and 2MHz.

Since LX node is always changing, when the NLD MOS is used as bottom switch, the junction cap of D_{sub} diode will cause some additional loss due to the charge and discharge at LX point.

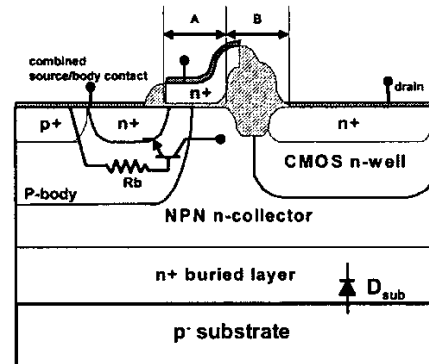
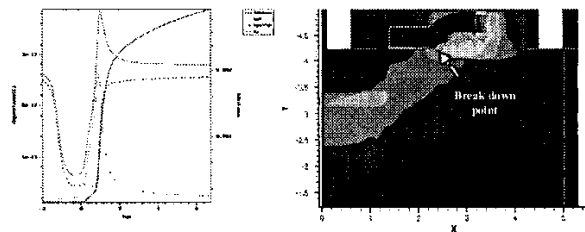
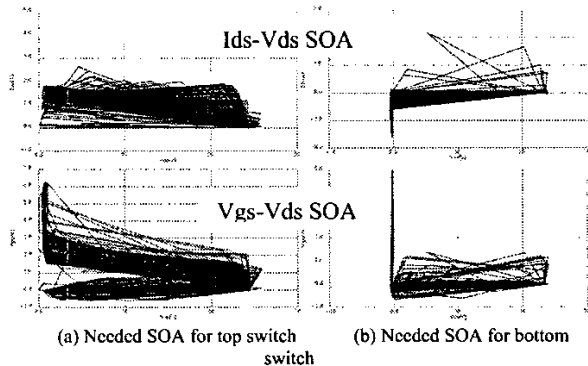
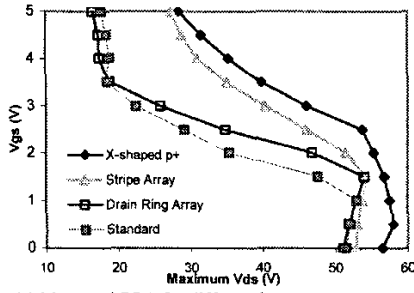


Fig. 4 Cross-section of NLD MOS used in the chip



(a) Parasitic components simulation (b) Breakdown voltage simulation
Fig. 5 Characteristics simulation by ISE for NLD MOS with $w=100u$, $L=0.5u$





(c) Measured SOA for different layout structure [7]
Fig. 6 SOA consideration for power switches

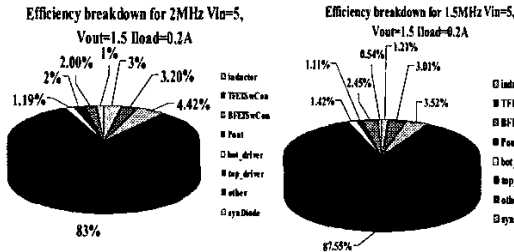


Fig. 7 Efficiency breakdown for 1.5MHz and 2MHz

E. Power stage design and separation with control part

In order to separate power stage and analog control part, several techniques are developed. Separated power ground and signal ground are used and connected only externally by bond wires to a single point on the PCB board. The parasitic inductance of bond wire helps to damp the noise injected from power stage. In the layout floor plan, noise sensitive blocks such as band-gap reference and compensator are placed far away from power stage and oscillating blocks. The noise from the input is another big issue since the input current is discontinuous. Due to parasitic inductance at the input power source, some noise will be generated at the input side. It may cause fault in the blocks that are connected with the input power source.

As mentioned before, since C_{gd} of the power switch is much larger than C_{gs} , a long holding period will increase the switching loss. At the same time, voltage spikes may be generated at LX and power ground due to the parasitic inductance of bond wires. The driver speed should be designed carefully so that the voltage spike will not break the power switches during turn on and turn off. Fig. 8 is the conventional gate driver (CGD). The charge current I_g is high at the beginning of the turn-on period, then drop down when V_g rise up. Fig. 9 is the typical waveform for the turn-on and turn-off of top switch. The whole turn on process can be divided into several stages: During $0-t_1$, driver charges C_{gs} to V_{th} , I_{ds} will stay at 0 and V_{ds} will keep at V_{in} (input power source voltage). During t_1-t_2 , driver charges C_{gs} to V_{GP} (Holding voltage). I_{ds} will rise from 0 to I_L and V_{ds} will keep at V_{in} . From t_2-t_3 , driver discharges C_{gd} and V_g will keep constant. V_{ds} will drop from V_{in} to 0. After t_3 , the switch will work in linear region. From the waveform we can see that I_{ds} rising speed is mainly determined by the time period t_1-t_2 . Fig. 10 is some simple modeling equations for the switching behavior. From Fig. 10, one can see that, I_{rr}

(Reverse recovery current) at turn on and $V_{ds,overvoltage}$ (Overshoot voltage) at turn off are determined by di_{ds}/dt .

In order to reduce I_{rr} and $V_{ds,overvoltage}$, the periods t_1-t_2 and t_5-t_6 are better to be longer. However, from Fig. 10, one can see that the switching loss is proportional to the turn on and turn off time. Considering this tradeoff, a multi-stage gate driver (MSGD) is designed in this chip. Fig. 11 is the basic concept of MSGD. For the different stages in Fig. 9, different gate charge currents I_g are applied. In the real implementation, the stages $0-t_1$ and t_1-t_2 use the same weak driver. After the current I_{ds} rises up to the inductor current, a strong driver is applied to pull up LX node quickly so that the overlap switching loss will be reduced. Fig 12 is the timing diagram for the high-speed multi-stage driver.

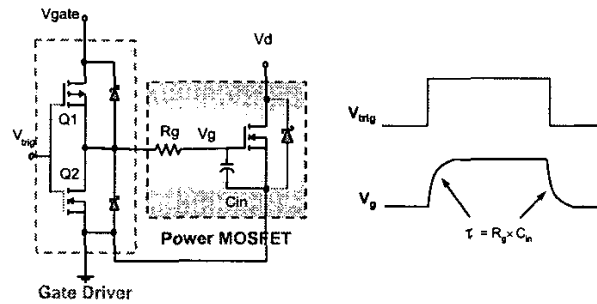
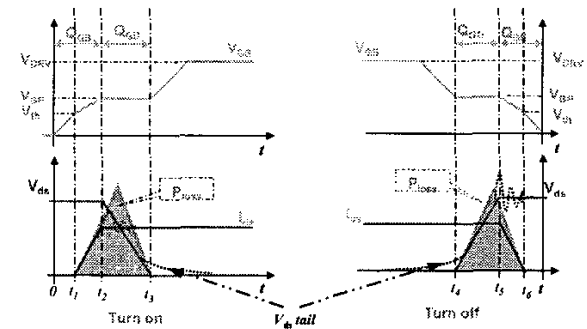


Fig. 8 Conventional gate drive (CGD)



(a) Typical turn on waveform (b) Typical turn off waveform
Fig. 9 timing diagram for the high-speed driver

$$I_{rr} = \sqrt{2 \cdot \tau \cdot I_{Load} \cdot \left(\frac{di}{dt}\right)_{on}} \quad \tau \text{ is the mean lifetime carrier for the diode}$$

$$V_{DS,Overvoltage} = L_s \cdot \left(\frac{di}{dt}\right)_{off}$$

$$P_{gate} = Q_G \cdot V_{drv} \cdot f_{sw} = C_G \cdot V_{drv}^2 \cdot f_{sw}$$

$$P_{conduction} = I_{Load}^2 \cdot R_{ds,on}$$

$$P_{switching} = \frac{1}{2} \cdot V_{in} \cdot i_L \cdot (t_{on} + t_{off})$$

Determined by the overlap of I_{ds} and V_{ds} in turn on and turn off

$$P_{loss_total} = P_{conduction} + P_{gate} + P_{switching}$$

Fig. 10 Simple modeling of switching behavior

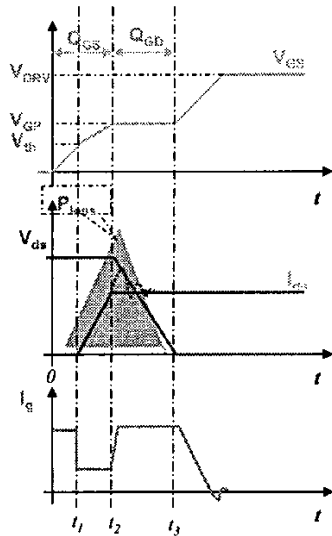


Fig. 11 Proposed multi-stage gate drive (MSGD)

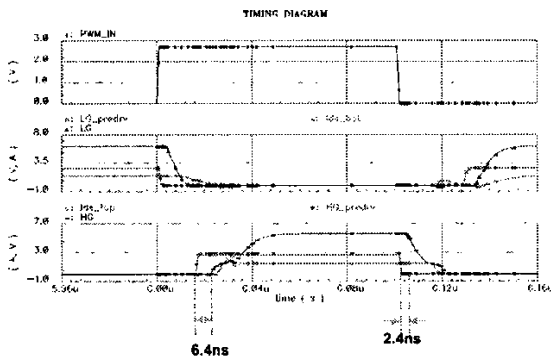


Fig. 12 Timing diagram of the multi-stage gate drive

III. EXPERIMENT RESULTS

The final silicon is fabricated and tested. Fig. 13 is the tested results for power on start-up. Fig. 14 is the tested results for a typical application.

IV. CONCLUSION

Several novel control concepts are proposed. Some important design issues for monolithic DC-DC switching converter ASIC design are identified and explored. The final silicon is fabricated and tested successfully.

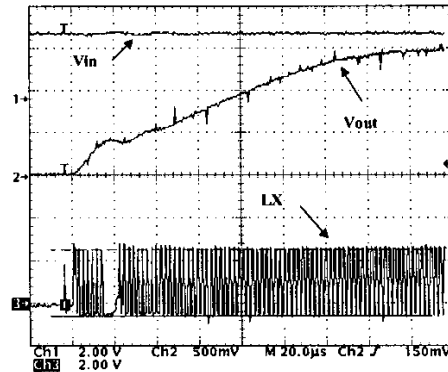


Fig. 13 Tested result for power on start-up Vin=3, Vout=1.5 Iload=200mA

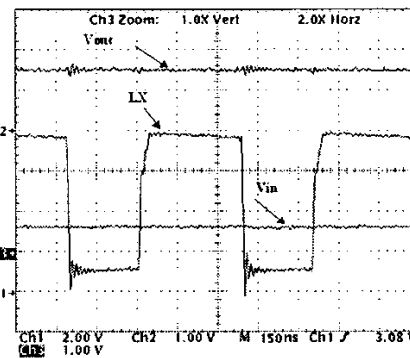


Fig. 14 Tested result for typical application Vin=3, Vout=1.5 Iload = 200mA

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